

TOSHIBA CMOS Digital Integrated Circuit Silicon Monolithic

TC83220-0020

TC83220-0020 Single-Chip CMOS LSI for FL (fluorescent) Calculator

The TOSHIBA printing/display calculator circuit TC83220-0020 is 10- or 12-digit calculator on single-chip CMOS LSI.

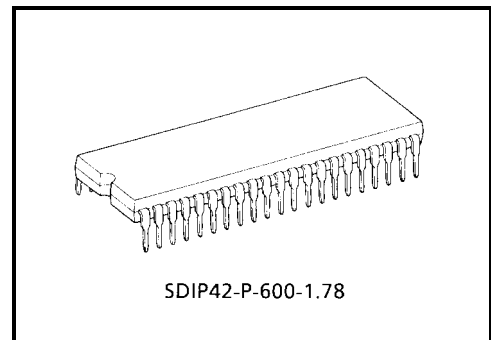
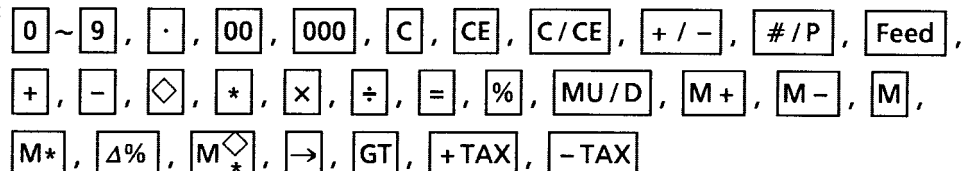
TC83220-0020 can drive the printing machine (M2158II/M2156II; EPSON) with magnet driver circuit, and can drive the fluorescent display tube with DC-DC converter.

It contains a 4 K-word ROM, a 256 × 4-bit RAM.

Features

Operational Features

- Print: 11 or 13 digits of data.
(including decimal point. 2 digits of operational symbol.)
3 digits of commas.
- Display: 10 or 12 digits of data. (including punctuation in each digit.)
1 digit of floating minus sign, memory load, error symbol.
3 digits of commas.
- Decimal output: Decimal set lock key controls output format.
Fixed decimal setting ("0", "1", "2", "3", "4", "6"), full floating decimal, and ADD mode.
- Key input buffer: 8 stages
- Function: 4 basic arithmetic functions (+, -, ×, ÷).
Repeat addition and subtraction.
Automatic constants in multiplication, division, percent calculation, calculations.
Automatic percent add-on and percent discount calculation.
Memory calculation.
Automatic accumulating calculation.
Gross margin profit calculation.
Delta percent calculation.
Tax calculation.
Grand total calculation.
Two-key rollover.
- Item counter: 0~999 count up or -999~0~999 count up/down by depressing of $\boxed{+}$, $\boxed{-}$ key.
- Punctuation: Commas for thousands on display
- Kinds of touch key:



Weight: 4.12 g (typ.)

- Kinds of lock key: “NP” printing mode selectable switch.
 “Σ” summation mode selectable switch.
 “5/4” “CUT” “UP” rounding switch.
 Fixed point mode selectable switch.
 “0”, “1”, “2”, “3”, “4”, “6”, “F”, “A”.
 “IC+” “IC±” item counter mode selectable switch.
 “GT” grand total memory selectable switch.
 “SET”, “CAL” tax memory selectable switch.
- Duty of display: Duty = 1/17.77
- Leading zero suppression
- Trailing zero suppression
- Tax calculation: +TAX key is calculation for included tax.
 -TAX key is calculation for excluded tax.
 SET selects set mode for tax rate.
 CAL selects normal calculation mode.
 Changing lock key from SET to CAL stores number of display to tax memory.
 Changing lock key from CAL to SET recalls tax rate to display from tax memory.
 Depression of +TAX following data key at CAL mode performs the calculating included tax.
 Depression of -TAX following data key at CAL mode performs the calculating excluded tax.

Electrical Features

- P-MOS output buffer with pull down resistor for direct driving of fluorescent display tube.
- Oscillator/clock generator internal to chip.
- Key board encoding internal to chip.
- Dual in line package.

Protection

- (1) In the overflow condition, all key except “C”, “C/CE”, “CE”, “Feed”, “→” key are inoperative.
- (2) Key bouncing protection (at 4 MHz clock)
 Key read in: 15 ms
 Key off: 40 ms

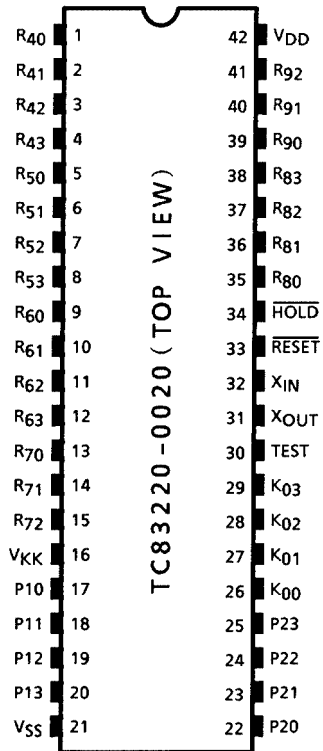
Function Select

- (1) “10/12” selectable with auto power off mode
 ON..... 10-digits calculated
 OFF..... 12-digits calculated

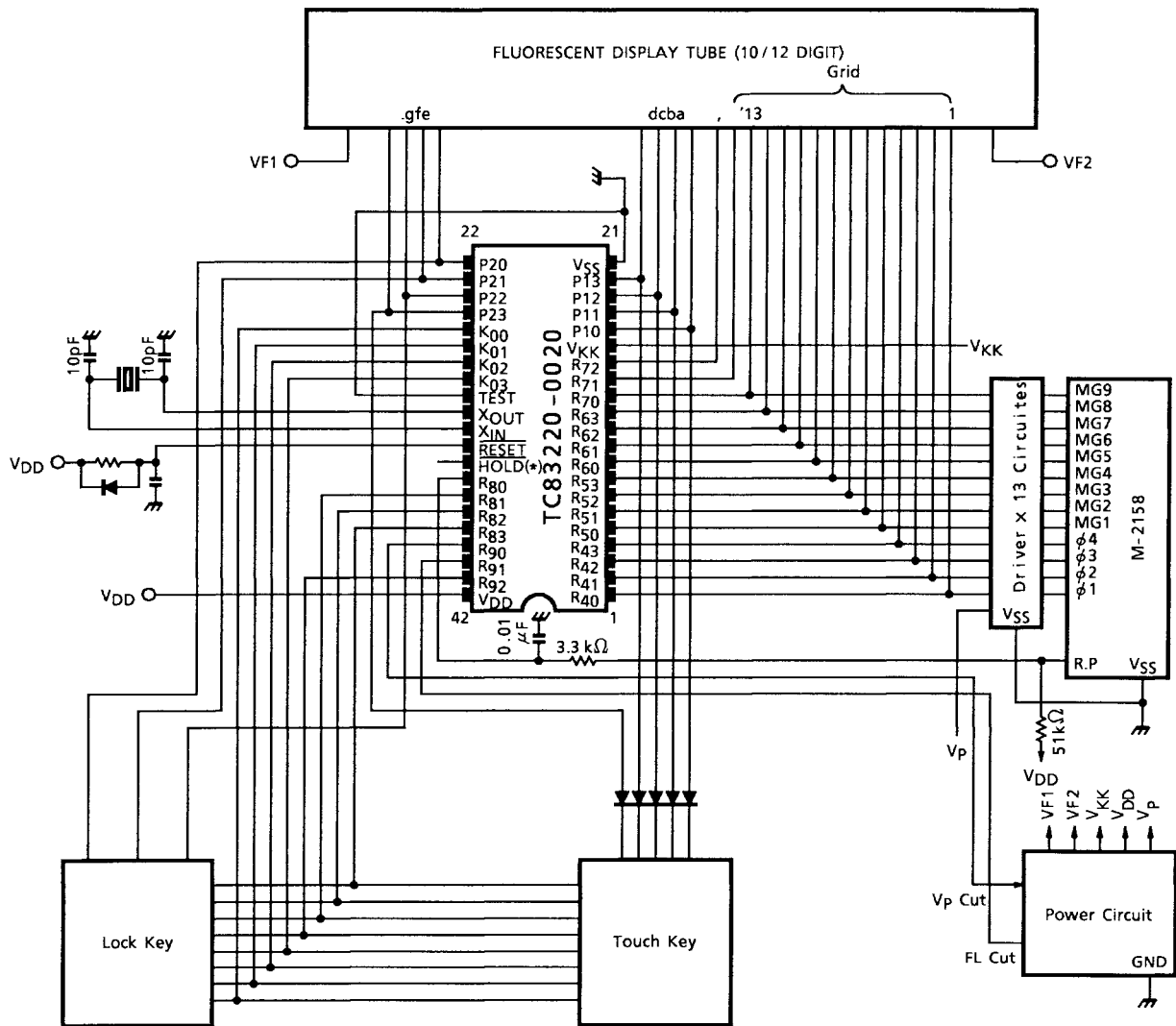
Speed of Calculation (at 4 MHz clock)

- | | | | |
|-----|------------------------|----------------------|----------|
| (1) | Addition | 1 + 1 + | 31.2 ms |
| (2) | Multiplication | × 999999999999 = | 26.8 ms |
| (3) | Division | 999999999999 ÷ 1 = | 100.6 ms |
| (4) | Memory calculation | 999999999999 ÷ 1 M + | 108.8 ms |
| (5) | Percentage calculation | 1 × 999999999999% | 35.2 ms |

Pin Assignment (top view)

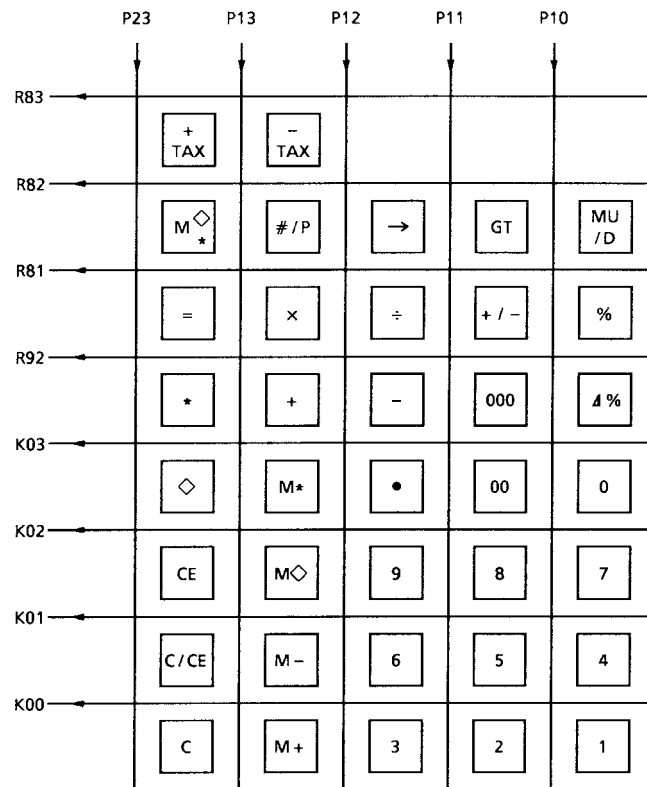


System Diagram

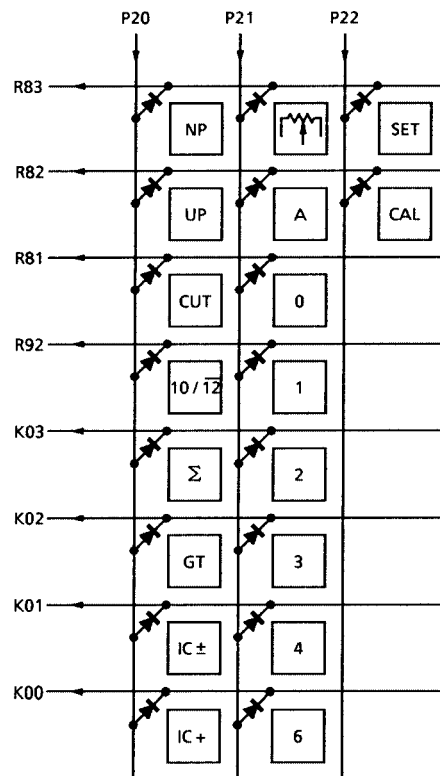


*: Connection to $\overline{\text{HOLD}}$ pin is shown in the following page.

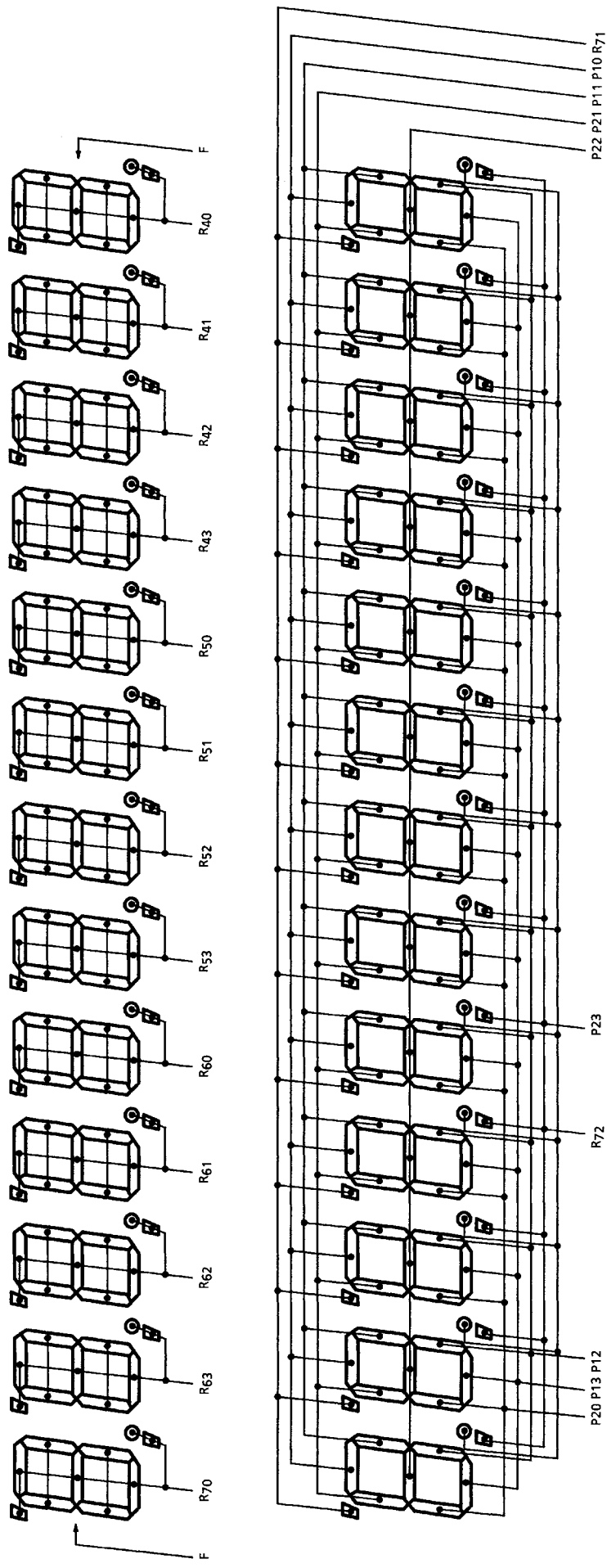
Key Connection



Touch Key



Lock Key

Connection of FL

Note 1: R70 digit (P20) of "E" data.

Note 2: R70 digit (P22) of "L" data.

Note 3: R70 digit (P23) of "M" data.

Note 4: R70 digit (P21) of "GT" data.

Operation Example

Key		Print	Display
TAB 4/5 IC 10/12 Σ GT MOD	Touch		
F 4/5 OFF 10 OFF OFF CAL	POWER ON	<PF>	
		C	
		<PF>	0.
	1+	1. +	1.
	2-	2. -	-1.
	◇	-1. ◇	-1.
	*	-1. *	
		<PF>	-1.
IC+	1+	1. +	1.
	2-	2. -	-1.
	◇	002	
		-1. ◇	-1.
	*	002	
		-1. *	
		<PF>	-1.
OFF	3×	3. ×	3.
	4÷	4. ÷	12.
	=	4. =	
		3. *	
		<PF>	3.
	5×	5. ×	5.
	6%	6. %	
		0.3 *	
		<PF>	0.3
	+	5.3 + %	
		<PF>	5.3
	2÷	2. ÷	2.
	3%	3. %	
		66.66666666 *	
		<PF>	66.66666666
	2 MU/D	2. M	2.
	3=	3. %	
		0.06185567 Δ *	
		2.06185567 *	
		<PF>	2.06185567
	2Δ%	2. Δ	2.
	3=	3. =	
		1. Δ *	
		50. Δ %	50.
		<PF>	

Note 5: <PF> Paper feed

Key		Print	Display
TAB 4/5 IC 10/12 Σ GT MOD	Touch		
F 4/5 OFF 10 Σ OFF CAL	3×	3. ×	3.
	4÷	4. ÷	12.
	=	4. =	
		3. +	
		<PF>	3.
	5×	5. ×	5.
	6%	6. %	
		0.3 +	
		<PF>	0.3
	+	5.3 + %	
		<PF>	5.3
	2÷	2. ÷	2.
	3%	3. %	
		66.66666666 +	
		<PF>	66.66666666
	2 MU/D	2. M	2.
	3=	3. %	
		0.06185567 Δ *	
		2.06185567 +	
		<PF>	2.06185567
	2Δ%	2. Δ	2.
	3=	3. =	
		1. Δ *	
		50. +	
		<PF>	50.
	*	122.0285223 *	
		<PF>	122.0285223
	GT	0. G ◊	0.
	GT	2. +	2.
	3+	3. +	5.
	*	5. G +	
		<PF>	5.
	3-	3. -	-3.
	4-	4. -	-7.
	5-	5. -	-12.
	*	-12. G +	
		<PF>	-12.
	GT	-7. G ◊	-7.
	GT	-7. G *	
		<PF>	-7.
	OFF	M+	M -7.
	C	0. C	M 0.

Note 5: <PF> Paper feed

Key		Print		Display	
TAB 4/5 IC 10/12 Σ GT MOD	Touch				
	M \diamond		<PF>	M	-7.
	M*		-7. M \diamond		
			-7. M *		
F 4/5 OFF 10 Σ OFF CAL			<PF>		-7.
	#/P		-7. \diamond		-7.
	2 #/P	#2			2.
	#/P		2. \diamond		2.
	0÷		0. ÷		0.
	=		0. =		
				
			0. *		
			<PF>	E	0.
	C		0. C		
			<PF>		0.
F CUT OFF 12 OFF OFF CAL	POWER ON		<PF>		
			C		
			<PF>		
	SET		0. %		
			<PF>		0.
	3				3.
	CAL		3. %		
			<PF>		0.
	C		0. C		
			<PF>		0.
	SET		3. %		
			<PF>		3.
	CAL				0.
	1560				1,560.
	+TAX		1,560.		
			46.8 Δ		
			1,606.8 *		
			<PF>		1,606.8
	+TAX		1,606.8 \diamond		
			48.204 Δ		
			1,655.004 *		
			<PF>		1,655.004
	1560				1,560.
	×		1,560. ×		1,560.
	78900				78,900.
	+TAX		78,900. =		
			123,084,000. \diamond		
			3,692,520. Δ		
			126,776,520. *		

Note 5: <PF> Paper feed

Key		Print	Display
TAB 4/5 IC 10/12 Σ GT MOD	Touch		
		<PF>	126,776,520.
	=		126,776,520.
	5		5.
	×	5. ×	5.
	+TAX		5.
	=	5. =	
		25. *	
		<PF>	25.
F CUT OFF 12 OFF OFF CAL	+TAX	25. ◊	
		0.75 Δ	
		25.75 *	
		<PF>	25.75
	=		25.75
	C	0. C	
		<PF>	0.
2	1560		1,560.
	+	1,560.00 +	1,560.00
	1100		1,100.
	+	1,100.00 +	2,660.00
	+TAX	2,660.00 ◊	
		79.80 Δ	
		2,739.80 *	
		<PF>	2,739.80
F	+TAX	2,739.80 ◊	
		82.194 Δ	
		2,821.994 *	
		<PF>	2,821.994
	980000000000		980,000,000,000.
	+TAX	980,000,000,000.	
		29,400,000,000. Δ	
		
		1.009400000000 *	
		<PF>	E 1.009400000000
	C	0. C	
		<PF>	0.
	1560		1560.
	+/-		-1,560.
	+TAX	-1,560.	
		-46.8 Δ	
		-1,606.8 *	
		<PF>	-1,606.8
	1560		1,560.
	-TAX	1,560.	

Note 5: <PF> Paper feed

Key		Print		Display
TAB 4/5 IC 10/12 Σ GT MOD	Touch			
F CUT OFF 12 OFF OFF CAL		-45,43689321 Δ		
		1,514.56310679 *		
		<PF>		1,514.56310679
	-TAX	1,514.56310679 ◊		
		-44.11348855 Δ		
		1,470.44961824 *		
		<PF>		1,470.44961824
	SET	3. %		
		<PF>		3.
	C			0.
	CAL	0. %		
		<PF>		0.
	SET	0. %		
		<PF>		0.
	1234			1,234.
	CAL	1,234. %		
		<PF>		0.
	980000000000			980,000,000,000.
	+TAX	980,000,000,000.		
			
		0. *		
		<PF>		E 0.
	C	0. C		
		<PF>		0.

Note 5: <PF> Paper feed

Maximum Ratings ($V_{SS} = 0\text{ V}$)

Characteristics	Symbol	Rating	Unit
Supply voltage 1	V_{DD}	-0.5~7	V
Supply voltage 2	V_{KK}	-40~+0.5	V
Input voltage	V_{IN}	-35~ $V_{DD} + 0.5$	V
Output voltage	V_{OUT}	-35~ $V_{DD} + 0.5$	V
Output current	I_{OUT}	-10	mA
Power dissipation ($T_{opr} = 70^{\circ}\text{C}$)	P_D	600	mW
Soldering temperature, time	T_{sld}	260 (10 s)	$^{\circ}\text{C}$
Storage temperature	T_{stg}	-55~125	$^{\circ}\text{C}$
Operating temperature	T_{opr}	0~40	$^{\circ}\text{C}$

Recommended Operating Conditions ($V_{SS} = 0\text{ V}$)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Max	Unit
Operating temperature	T_{opr}	—	—	0	40	$^{\circ}\text{C}$
Supply voltage	V_{DD}	—	—	4.5	6	V
Supply voltage (FL)	V_{KK}	—	—	-30	-15	V
Supply voltage (hold)	V_{DDH}	—	—	2	6	V
Input high voltage (except schmitt circuit input)	V_{IH1}	—	$V_{DD} \geq 4.5\text{ V}$	$V_{DD} \times 0.7$	V_{DD}	V
Input high voltage (schmitt circuit input)	V_{IH2}	—		$V_{DD} \times 0.75$	V_{DD}	V
Input high voltage	V_{IH3}	—	$V_{DD} < 4.5\text{ V}$	$V_{DD} \times 0.9$	V_{DD}	V
Input low voltage (except schmitt circuit input)	V_{IL1}	—	$V_{DD} \geq 4.5\text{ V}$	V_{KK}	$V_{DD} \times 0.3$	V
Input low voltage (schmitt circuit input)	V_{IL2}	—		V_{KK}	$V_{DD} \times 0.25$	V
Input low voltage	V_{IL3}	—	$V_{DD} < 4.5\text{ V}$	V_{KK}	$V_{DD} \times 0.1$	V
Output voltage (source open drain)	V_{OUT}	—	—	$V_{DD} - 35$	V_{DD}	V
Clock high pulse width (Note 6)	T_{WCH}	—	$V_{IN} = V_{IH}$	80	—	ns
Clock low pulse width (Note 6)	T_{WCL}	—	$V_{IN} = V_{IL}$	80	—	ns

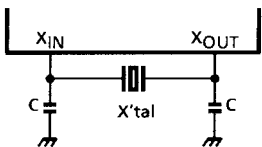
Note 6: In case of the external clock operation.

Electrical Characteristics

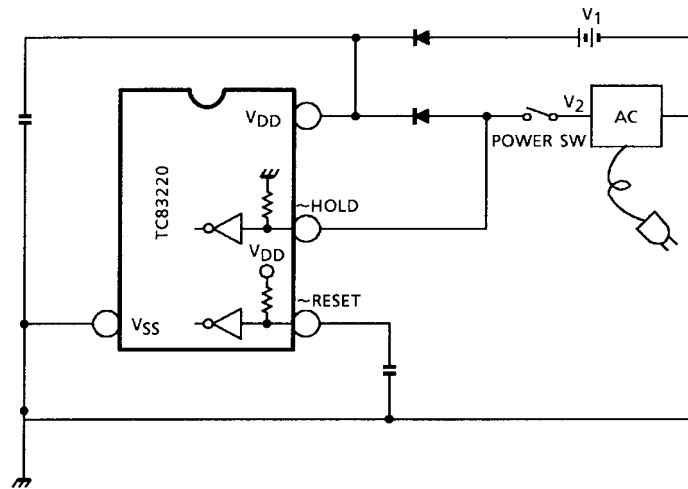
DC Characteristics ($V_{SS} = 0\text{ V}$, $V_{DD} \pm 10\%$, $T_{opr} = 0\sim 40^\circ\text{C}$)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Hysteresis voltage (schmitt circuit input)	V_{HS}	—	—	—	0.7	—	V
Input current ($\overline{\text{RESET}}$, $\overline{\text{HOLD}}$, $\overline{\text{TEST}}$)	I_{IN}	—	$V_{DD} = 5.5\text{ V}$, $V_{IN} = 5.5/0\text{ V}$	—	—	± 50	μA
Output leak current (source open drain)	I_{LO}	—	$V_{DD} = 5.5\text{ V}$, $V_{OUT} = -32\text{ V}$	—	—	-10	μA
Output high voltage (P1~P2, R4~R9)	V_{OH}	—	$V_{DD} = 4.5\text{ V}$, $I_{OH} = -6\text{ mA}$	2.4	—	—	V
Input pull down resistor (K0, R7~R9)	R_{IN}	—	$V_{DD} = 5.5\text{ V}$, $V_{KK} = -30\text{ V}$	—	100	—	$\text{k}\Omega$
Pull down resistor (source open drain)	R_{KK}	—		50	80	200	$\text{k}\Omega$
Operating supply current	$I_{DD\ 0}$	—	V_{DD} (V_{DDH}) 5.5 V , $f_c = 4\text{ MHz}$, $V_{IN} = 5.3/0.2\text{ V}$	—	3	6	mA
Supply current (after clear)	$I_{KK\ 1}$	—	$V_{KK} = -30\text{ V}$, $f_c = 4\text{ MHz}$	—	0.6	0.9	mA
Supply current (shown full digits)	$I_{KK\ 2}$	—		—	3.5	6	mA
Holding supply current	$I_{DD\ H}$	—	$V_{DD} = 5.5\text{ V}$	—	0.5	10	μA

Oscillation Characteristics ($T_{opr} = 0\sim 40^\circ\text{C}$, $V_{DD} = 4.5\sim 6.0\text{ V}$)

Circuit	Test Condition	Min	Typ.	Max	Unit
	$C = 10\text{ pF}$ $X'tal$ (or ceramic) = 4 MHz	—	4	—	MHz

The Proposal of Outer Circuit for Tax Rate Holding with Back-Up Battery



Note 7: $V_1 = 3\text{ V}$: Battery supply

$V_2 = 5\text{ V}$: AC supply

(\sim HOLD pin is pulled down in the LSI, but normally pulled up to VDD.)
 (\sim RESET pin is pulled up to VDD.)

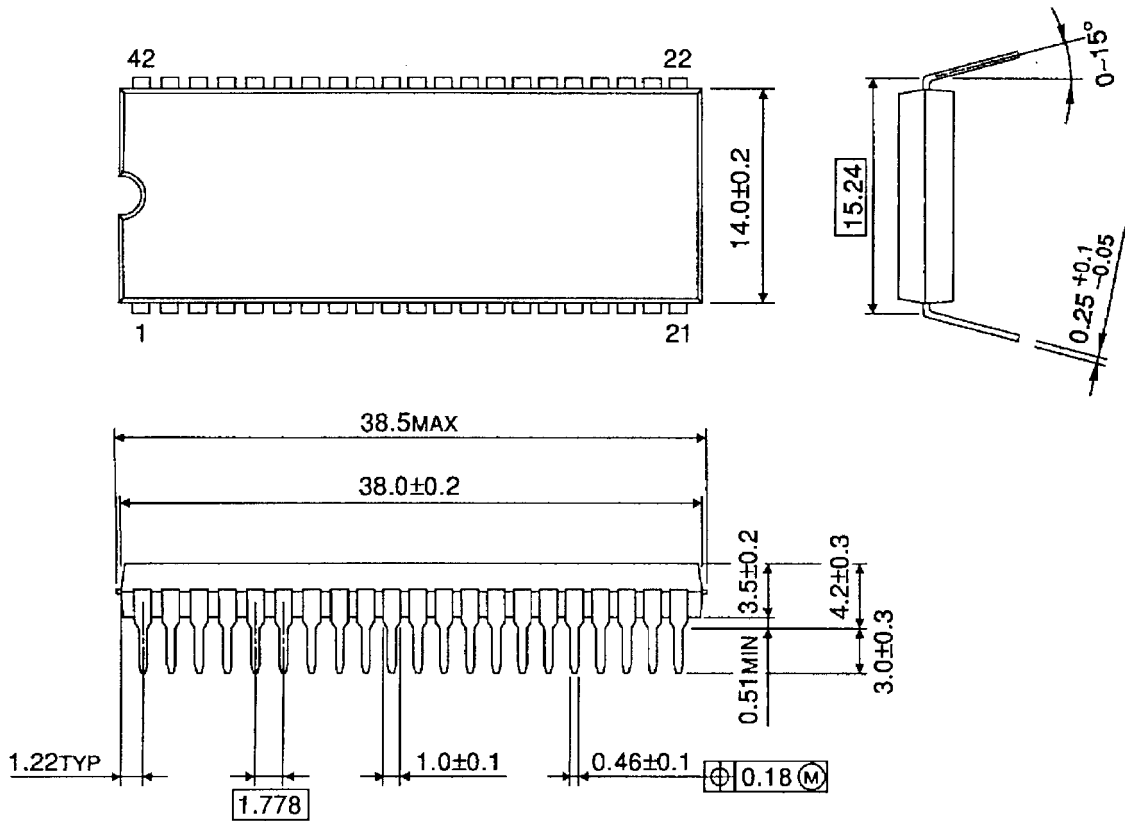
- (1) Setting POWER SW to ON, V_2 is supplied to VDD pin, and also to HOLD pin. Then calculator operates normally.
- (2) Setting POWER SW from ON to OFF, V_1 is supplied to VDD pin and VSS is supplied to HOLD pin. Under this connection, TAX RATE is held.
- (3) Setting POWER SW to ON, V_2 is supplied to VDD pin, and also to HOLD pin. Then calculator operates normally with TAX RATE to be held.

Note 8: V_1 (battery) should be supplied to the circuit after V_2 (AC) supply, because of prevention from exhaustion of battery and abnormal operation.

Package Dimensions

SDIP42-P-600-1.78

Unit : mm



Weight: 4.12 g (typ.)

RESTRICTIONS ON PRODUCT USE

000707EBA

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