TOSHIBA CMOS Digital Integrated Circuit   Silicon Monolithic

TC83220-0020

TC83220-0020 Single-Chip CMOS LSI for FL (fluorescent) Calculator

The TOSHIBA printing/display calculator circuit TC83220-0020 is 10- or 12-digit calculator on single-chip CMOS LSI.
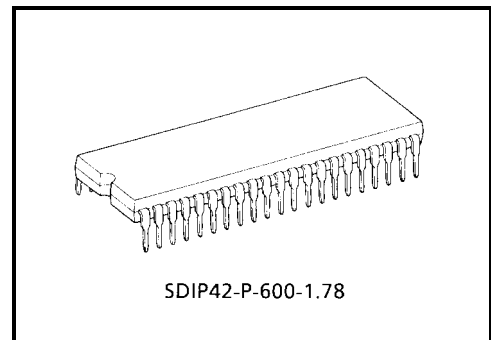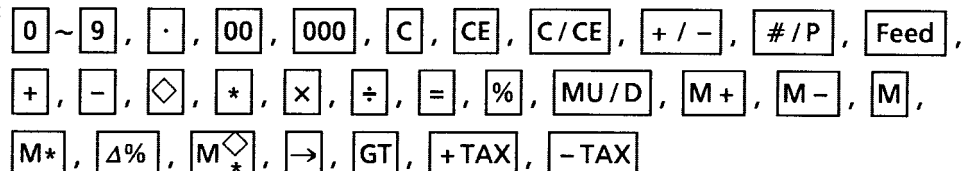
TC83220-0020 can drive the printing machine (M2158II/ M2156II; EPSON) with magnet driver circuit, and can drive the fluorescent display tube with DC-DC converter.

It contains a 4 K-word ROM, a 256 × 4-bit RAM.

SDIP42-P-600-1.78

Weight: 4.12 g (typ.)

Features

Operational Features

- Print: 11 or 13 digits of data.
  (including decimal point. 2 digits of operational symbol.)
  3 digits of commas.
- Display: 10 or 12 digits of data. (including punctuation in each digit.)
  1 digit of floating minus sign, memory load, error symbol.
  3 digits of commas.
- Decimal output: Decimal set lock key controls output format.
  Fixed decimal setting ("0", "1", "2", "3", "4", "6"), full floating decimal, and ADD mode.
- Key input buffer: 8 stages
- Function: 4 basic arithmetic functions (+, −, ×, ÷).
  Repeat addition and subtraction.
  Automatic constants in multiplication, division, percent calculation, calculations.
  Automatic percent add-on and percent discount calculation.
  Memory calculation.
  Automatic accumulating calculation.
  Gross margin profit calculation.
  Delta percent calculation.
  Tax calculation.
  Grand total calculation.
  Two-key rollover.
- Item counter: 0~999 count up or −999~0~999 count up/down by depressing of $\boxed{+}$, $\boxed{-}$ key.
- Punctuation: Commas for thousands on display
- Kinds of touch key: $\boxed{0}$~$\boxed{9}$, $\boxed{\cdot}$, $\boxed{00}$, $\boxed{000}$, $\boxed{C}$, $\boxed{CE}$, $\boxed{C/CE}$, $\boxed{+/-}$, $\boxed{\#/P}$, $\boxed{Feed}$, $\boxed{+}$, $\boxed{-}$, $\boxed{\diamondsuit}$, $\boxed{*}$, $\boxed{\times}$, $\boxed{\div}$, $\boxed{=}$, $\boxed{\%}$, $\boxed{MU/D}$, $\boxed{M+}$, $\boxed{M-}$, $\boxed{M}$, $\boxed{M*}$, $\boxed{\Delta\%}$, $\boxed{M^{\diamondsuit}_{*}}$, $\boxed{\rightarrow}$, $\boxed{GT}$, $\boxed{+TAX}$, $\boxed{-TAX}$

- Kinds of lock key: "NP" printing mode selectable switch.

  "Σ" summation mode selectable switch.

  "5/4" "CUT" "UP" rounding switch.

  Fixed point mode selectable switch.

  "0", "1", "2", "3", "4", "6", "F", "A".

  "IC+" "IC±" item counter mode selectable switch.

  "GT" grand total memory selectable switch.

  "SET", "CAL" tax memory selectable switch.

- Duty of display: Duty = 1/17.77
- Leading zero suppression
- Trailing zero suppression
- Tax calculation: $\boxed{+TAX}$ key is calculation for included tax.

  $\boxed{-TAX}$ key is calculation for excluded tax.

  $\boxed{SET}$ selects set mode for tax rate.

  $\boxed{CAL}$ selects normal calculation mode.

  Changing lock key from $\boxed{SET}$ to $\boxed{CAL}$ stores number of display to tax memory.

  Changing lock key from $\boxed{CAL}$ to $\boxed{SET}$ recalls tax rate to display from tax memory.

  Depression of $\boxed{+TAX}$ following data key at CAL mode performs the calculating included tax.

  Depression of $\boxed{-TAX}$ following data key at CAL mode performs the calculating excluded tax.

Electrical Features

- P-MOS output buffer with pull down resistor for direct driving of fluorescent display tube.
- Oscillator/clock generator internal to chip.
- Key board encoding internal to chip.
- Dual in line package.

Protection

(1) In the overflow condition, all key except "C", "C/CE", "CE", "Feed", "→" key are inoperative.

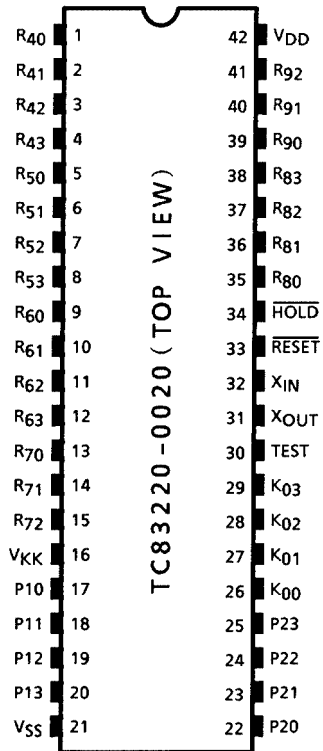(2) Key bouncing protection (at 4 MHz clock)

Key read in: 15 ms

Key off: 40 ms

Function Select

(1) "10/12" selectable with auto power off mode

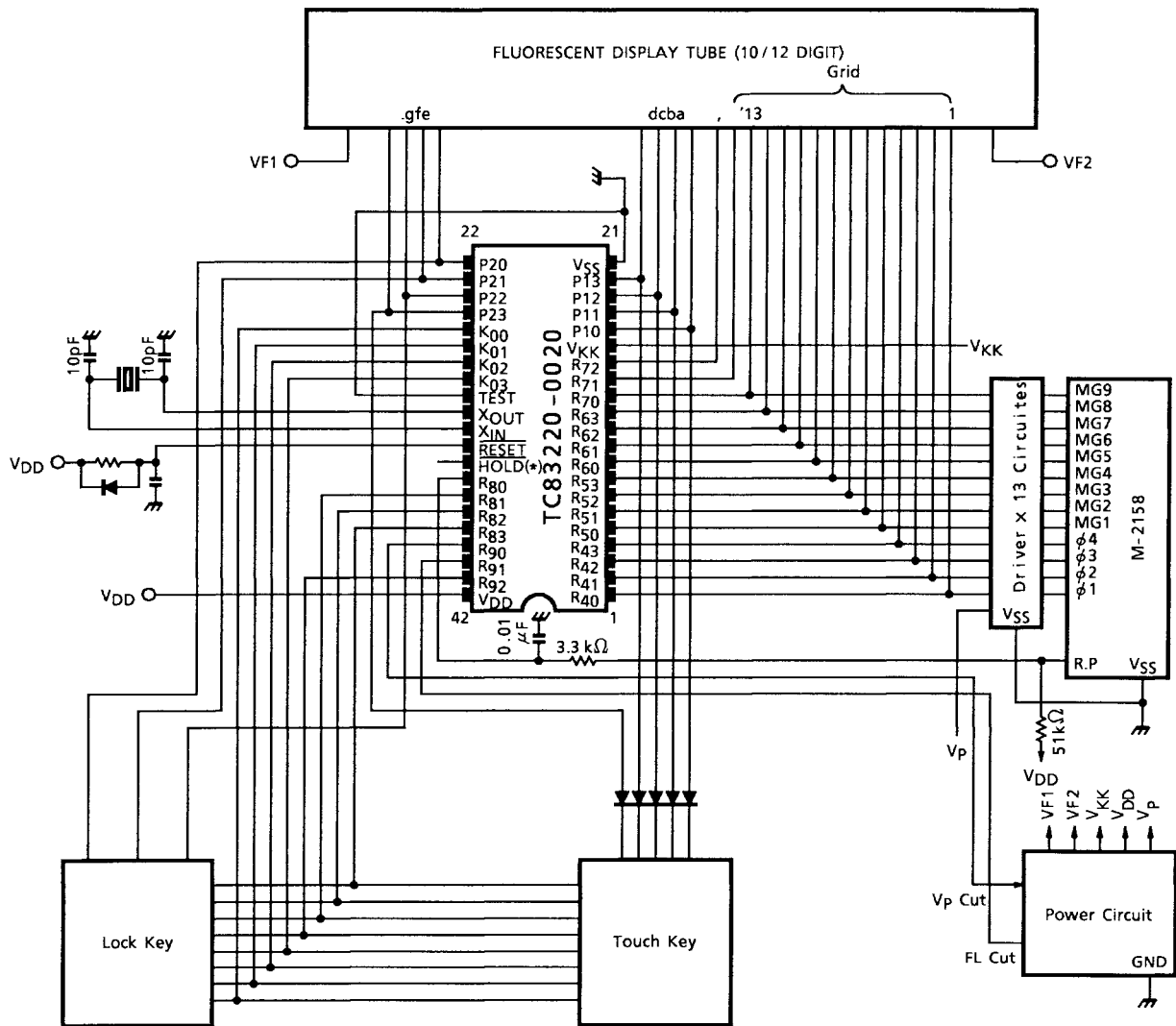ON........... 10-digits calculated

OFF......... 12-digits calculated

Speed of Calculation (at 4 MHz clock)

(1)	Addition	$1 + 1 +$	31.2 ms
(2)	Multiplication	$\times 999999999999 =$	26.8 ms
(3)	Division	$999999999999 \div 1 =$	100.6 ms
(4)	Memory calculation	$999999999999 \div 1\ M +$	108.8 ms
(5)	Percentage calculation	$1 \times 999999999999\%$	35.2 ms

Pin Assignment (top view)

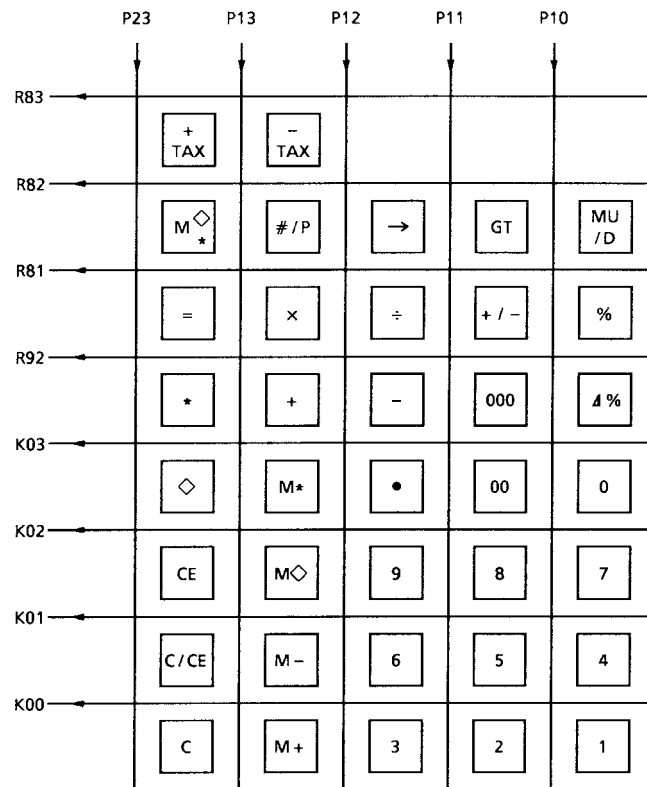| Pin		TC83220-0020 (TOP VIEW)		Pin
R_{40}	1		42	V_{DD}
R_{41}	2		41	R_{92}
R_{42}	3		40	R_{91}
R_{43}	4		39	R_{90}
R_{50}	5		38	R_{83}
R_{51}	6		37	R_{82}
R_{52}	7		36	R_{81}
R_{53}	8		35	R_{80}
R_{60}	9		34	$\overline{HOLD}$
R_{61}	10		33	$\overline{RESET}$
R_{62}	11		32	X_{IN}
R_{63}	12		31	X_{OUT}
R_{70}	13		30	TEST
R_{71}	14		29	K_{03}
R_{72}	15		28	K_{02}
V_{KK}	16		27	K_{01}
P10	17		26	K_{00}
P11	18		25	P23
P12	19		24	P22
P13	20		23	P21
V_{SS}	21		22	P20

System Diagram

*: Connection to $\overline{\text{HOLD}}$ pin is shown in the following page.
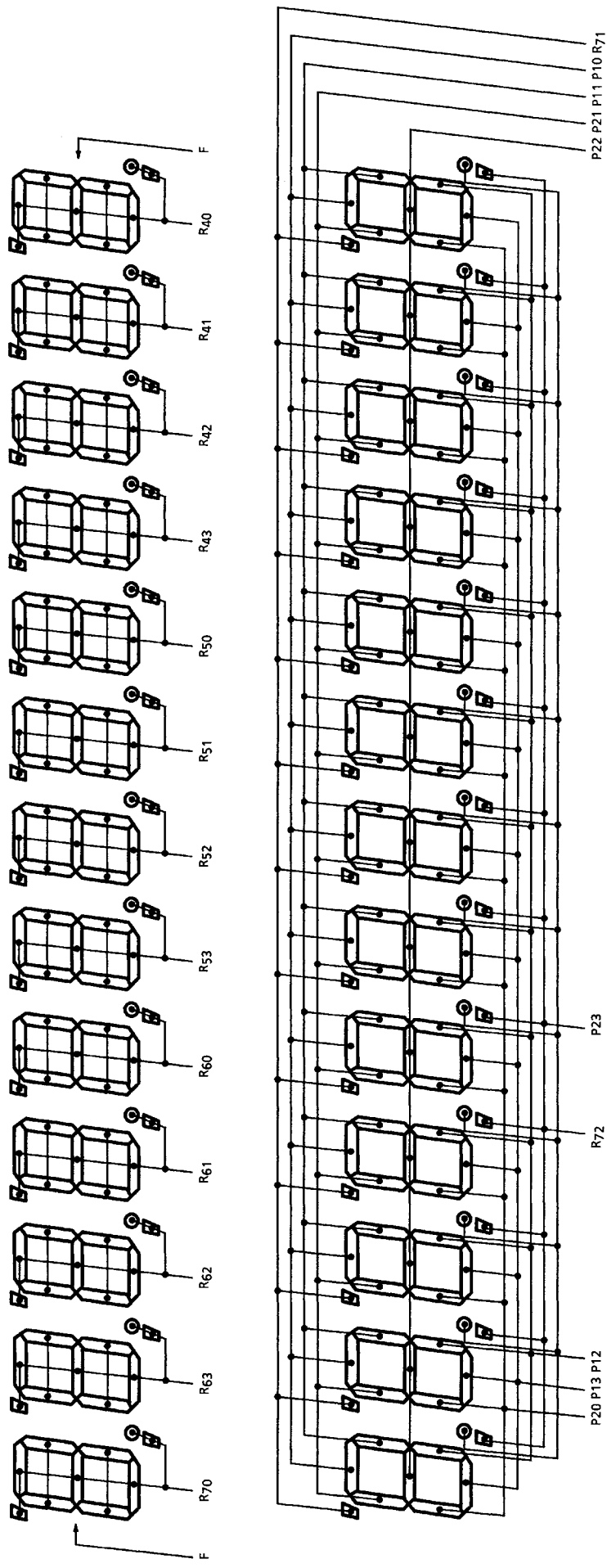
Key Connection

Touch Key
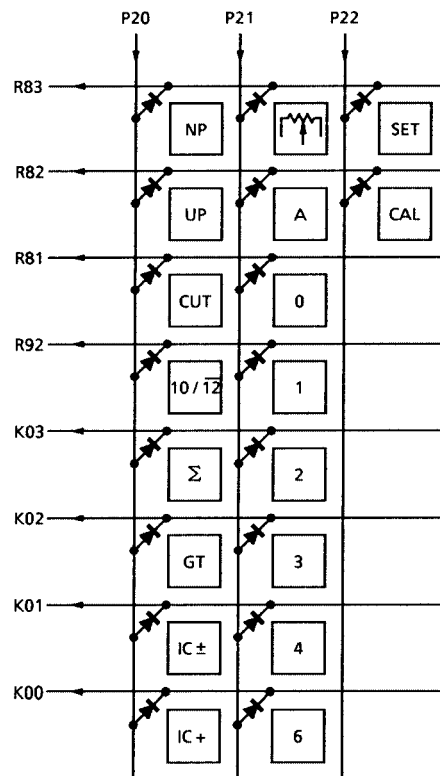
Lock Key

Connection of FL

Note 1: R_{70} digit (P20) of "E" data.

Note 2: R_{70} digit (P22) of "—" data.

Note 3: R_{70} digit (P23) of "M" data.

Note 4: R_{70} digit (P21) of "GT" data.

Operation Example

Key		Print		Display
TAB 4/5 IC 10/12 Σ GT MOD	Touch			
F 4/5 OFF 10 OFF OFF CAL	POWER ON			
		`<PF>`		
		C		
		`<PF>`		0.
	1+	1. +		1.
	2−	2. −		−1.
	◊	−1. ◊		−1.
	*	−1. *		−1.
		`<PF>`		−1.
IC+	1+	1. +		1.
	2−	2. −		−1.
	◊	002		
		−1. ◊		−1.
	*	002		
		−1. *		
		`<PF>`		−1.
OFF	3×	3. ×		3.
	4÷	4. ÷		12.
	=	4. =		
		3. *		
		`<PF>`		3.
	5×	5. ×		5.
	6%	6. %		
		0.3 *		
		`<PF>`		0.3
	+	5.3 + %		5.3
		`<PF>`		5.3
	2÷	2. ÷		2.
	3%	3. %		
		66.66666666 *		
		`<PF>`		66.66666666
	2 MU/D	2. M		2.
	3=	3. %		
		0.06185567 Δ *		
		2.06185567 *		
		`<PF>`		2.06185567
	2Δ%	2. Δ		2.
	3=	3. =		
		1. Δ *		
		50. Δ %		50.
		`<PF>`		

Note 5:   `<PF>` .... Paper feed

Key						Print	Display
TAB 4/5	IC 10/12	Σ	GT	MOD	Touch		
F 4/5 OFF 10	Σ		OFF	CAL	3×	3. ×	3.
					4÷	4. ÷	12.
					=	4. =	
						3. +	
						<PF>	3.
					5×	5. ×	5.
					6%	6. %	
						0.3 +	
						<PF>	0.3
					+	5.3 + %	
						<PF>	5.3
					2÷	2. ÷	2.
					3%	3. %	
						66.66666666 +	
						<PF>	66.66666666
					2 MU/D	2. M	2.
					3=	3. %	
						0.06185567 Δ *	
						2.06185567 +	
						<PF>	2.06185567
					2Δ%	2. Δ	2.
					3=	3. =	
						1. Δ *	
						50. +	
						<PF>	50.
					*	122.0285223 *	
						<PF>	122.0285223
					GT	0. G ◊	0.
			GT		2+	2. +	2.
					3+	3. +	5.
					*	5. G +	
						<PF>	5.
					3−	3. −	−3.
					4−	4. −	−7.
					5−	5. −	−12.
					*	−12. G +	
						<PF>	−12.
					GT	−7. G ◊	−7.
					GT	−7. G *	
						<PF>	−7.
			OFF		M+	−7. M +	M −7.
					C	0. C	M 0.

Note 5: <PF> .... Paper feed

Key		Print	Display
TAB 4/5 IC 10/12 Σ GT MOD	Touch		
	M◊	`<PF>`	M −7.
	M*	−7. M ◊	
		−7. M *	
F 4/5 OFF 10 Σ OFF CAL		`<PF>`	−7.
	#/P	−7. ◊	−7.
	2 #/P	#2	2.
	#/P	2. ◊	2.
	0÷	0. ÷	0.
	=	0. =	
		. . . .	
		0. *	
		`<PF>`	E 0.
	C	0. C	
		`<PF>`	0.
F CUT OFF 12 OFF OFF CAL	POWER ON	`<PF>`	
		C	
		`<PF>`	
	SET	0. %	
		`<PF>`	0.
	3		3.
	CAL	3. %	
		`<PF>`	0.
	C	0. C	
		`<PF>`	0.
	SET	3. %	
		`<PF>`	3.
	CAL		0.
	1560		1,560.
	+TAX	1,560.	
		46.8 Δ	
		1,606.8 *	
		`<PF>`	1,606.8
	+TAX	1,606.8 ◊	
		48.204 Δ	
		1,655.004 *	
		`<PF>`	1,655.004
	1560		1,560.
	×	1,560. ×	1,560.
	78900		78,900.
	+TAX	78,900. =	
		123,084,000. ◊	
		3,692,520. Δ	
		126,776,520. *	

Note 5: `<PF>` .... Paper feed

Key		Print		Display
TAB 4/5 IC 10/12 Σ GT MOD	Touch			
		<PF>		126,776,520.
	=			126,776,520.
	5			5.
	×	5. ×		5.
	+TAX			5.
	=	5. =		
		25. *		
		<PF>		25.
F CUT OFF 12 OFF OFF CAL	+TAX	25. ◊		
		0.75 Δ		
		25.75 *		
		<PF>		25.75
	=			25.75
	C	0. C		
		<PF>		0.
2	1560			1,560.
	+	1,560.00 +		1,560.00
	1100			1,100.
	+	1,100.00 +		2,660.00
	+TAX	2,660.00 ◊		
		79.80 Δ		
		2,739.80 *		
		<PF>		2,739.80
F	+TAX	2,739.80 ◊		
		82.194 Δ		
		2,821.994 *		
		<PF>		2,821.994
	980000000000			980,000,000,000.
	+TAX	980,000,000,000.		
		29,400,000,000. Δ		
		....		
		1.00940000000 *		
		<PF>		E 1.00940000000
	C	0. C		
		<PF>		0.
	1560			1560.
	+/−			−1,560.
	+TAX	−1,560.		
		−46.8 Δ		
		−1,606.8 *		
		<PF>		−1,606.8
	1560			1,560.
	−TAX	1,560.		

Note 5: <PF> .... Paper feed

Key								Touch	Print		Display
TAB	4/5	IC	10/12	Σ		GT	MOD				
F	CUT	OFF	12	OFF		OFF	CAL		−45,43689321　Δ		
									1,514.56310679　　*		
									<PF>		1,514.56310679
								−TAX	1,514.56310679　◊		
									−44.11348855　Δ		
									1,470.44961824　　*		
									<PF>		1,470.44961824
								SET	3.　　%		
									<PF>		3.
								C			0.
								CAL	0.　　%		
									<PF>		0.
								SET	0.　　%		
									<PF>		0.
								1234			1,234.
								CAL	1,234.　　%		
									<PF>		0.
								980000000000			980,000,000,000.
								+TAX	980,000,000,000.		
									....		
									0.　　*		
									<PF>	E	0.
								C	0.　C		
									<PF>		0.

Note 5:　<PF> .... Paper feed

Maximum Ratings (V$_{SS}$ = 0 V)

Characteristics	Symbol	Rating	Unit
Supply voltage 1	V$_{DD}$	$-0.5 \sim 7$	V
Supply voltage 2	V$_{KK}$	$-40 \sim +0.5$	V
Input voltage	V$_{IN}$	$-35 \sim V_{DD} + 0.5$	V
Output voltage	V$_{OUT}$	$-35 \sim V_{DD} + 0.5$	V
Output current	I$_{OUT}$	-10	mA
Power dissipation (T$_{opr}$ = 70°C)	P$_D$	600	mW
Soldering temperature, time	T$_{sld}$	260 (10 s)	°C
Storage temperature	T$_{stg}$	$-55 \sim 125$	°C
Operating temperature	T$_{opr}$	$0 \sim 40$	°C

Recommended Operating Conditions (V$_{SS}$ = 0 V)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Max	Unit
Operating temperature	T$_{opr}$	—	—	0	40	°C
Supply voltage	V$_{DD}$	—	—	4.5	6	V
Supply voltage (FL)	V$_{KK}$	—	—	-30	-15	V
Supply voltage (hold)	V$_{DDH}$	—	—	2	6	V
Input high voltage (except schmitt circuit input)	V$_{IH1}$	—	V$_{DD} \geqq 4.5$ V	V$_{DD} \times$ 0.7	V$_{DD}$	V
Input high voltage (schmitt circuit input)	V$_{IH2}$	—		V$_{DD} \times$ 0.75	V$_{DD}$	V
Input high voltage	V$_{IH3}$	—	V$_{DD} < 4.5$ V	V$_{DD} \times$ 0.9	V$_{DD}$	V
Input low voltage (except schmitt circuit input)	V$_{IL1}$	—	V$_{DD} \geqq 4.5$ V	V$_{KK}$	V$_{DD} \times$ 0.3	V
Input low voltage (schmitt circuit input)	V$_{IL2}$	—		V$_{KK}$	V$_{DD} \times$ 0.25	V
Input low voltage	V$_{IL3}$	—	V$_{DD} < 4.5$ V	V$_{KK}$	V$_{DD} \times$ 0.1	V
Output voltage (source open drain)	V$_{OUT}$	—	—	V$_{DD} -$ 35	V$_{DD}$	V
Clock high pulse width (Note 6)	T$_{WCH}$	—	V$_{IN} = V_{IH}$	80	—	ns
Clock low pulse width (Note 6)	T$_{WCL}$	—	V$_{IN} = V_{IL}$	80	—	ns
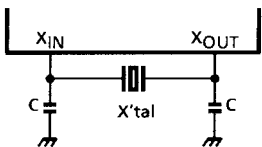
Note 6: In case of the external clock operation.

Electrical Characteristics

DC Characteristics (V_{SS} = 0 V, V_{DD} ± 10%, T_{opr} = 0~40°C)

Characteristics	Symbol	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Hysteresis voltage (schmitt circuit input)	V_{HS}	—	—	—	0.7	—	V
Input current ($\overline{RESET}$, $\overline{HOLD}$, $\overline{TEST}$)	I_{IN}	—	V_{DD} = 5.5 V, V_{IN} = 5.5/0 V	—	—	±50	μA
Output leak current (source open drain)	I_{LO}	—	V_{DD} = 5.5 V, V_{OUT} = −32 V	—	—	−10	μA
Output high voltage (P1~P2, R_4~R_9)	V_{OH}	—	V_{DD} = 4.5 V, I_{OH} = −6 mA	2.4	—	—	V
Input pull down resistor (K_0, R_7~R_9)	R_{IN}	—	V_{DD} = 5.5 V, V_{KK} = −30 V	—	100	—	kΩ
Pull down resistor (source open drain)	R_{KK}	—		50	80	200	kΩ
Operating supply current	I_{DD} 0	—	V_{DD} (V_{DDH}) 5.5 V, f_c = 4 MHz, V_{IN} = 5.3/0.2 V	—	3	6	mA
Supply current (after clear)	I_{KK} 1	—	V_{KK} = −30 V, f_c = 4 MHz	—	0.6	0.9	mA
Supply current (shown full digits)	I_{KK} 2	—		—	3.5	6	mA
Holding supply current	I_{DD} H	—	V_{DD} = 5.5 V	—	0.5	10	μA

Oscillation Characteristics (T_{opr} = 0~40°C, V_{DD} = 4.5~6.0 V)

Circuit	Test Condition	Min	Typ.	Max	Unit
	C = 10 pF X'tal (or ceramic) = 4 MHz	—	4	—	MHz

The Proposal of Outer Circuit for Tax Rate Holding with Back-Up Battery
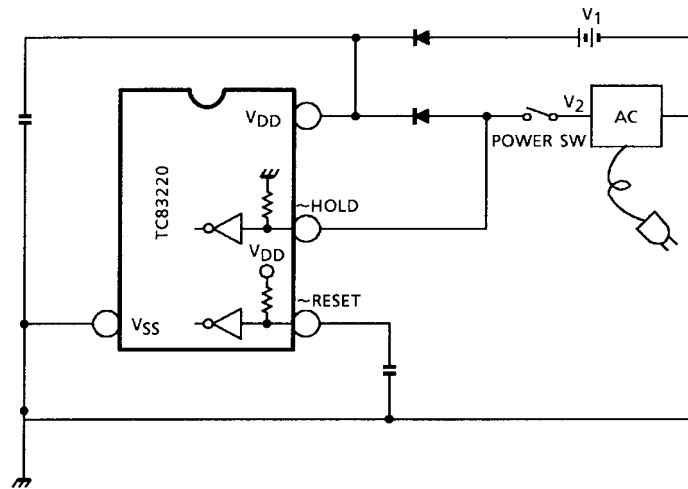
Note 7: $V_1 = 3$ V: Battery supply

$V_2 = 5$ V: AC supply

$\left[\begin{array}{l}\text{~HOLD pin is pulled down in the LSI, but normally pulled up to } V_{DD}.\\ \text{~RESET pin is pulled up to } V_{DD}.\end{array}\right]$

(1)   Setting POWER SW to ON, V_2 is supplied to V_{DD} pin, and also to HOLD pin.
Then calculator operates normally.

(2)   Setting POWER SW from ON to OFF, V_1 is supplied to V_{DD} pin and V_{SS} is supplied to HOLD pin.
Under this connection, TAX RATE is held.

(3)   Setting POWER SW to ON, V_2 is supplied to V_{DD} pin, and also to HOLD pin.
Then calculator operates normally with TAX RATE to be held.

Note 8: V_1 (battery) should be supplied to the circuit after V_2 (AC) supply, because of prevention from
exhaustion of battery and abnormal operation.

Package Dimensions

SDIP42-P-600-1.78   Unit : mm
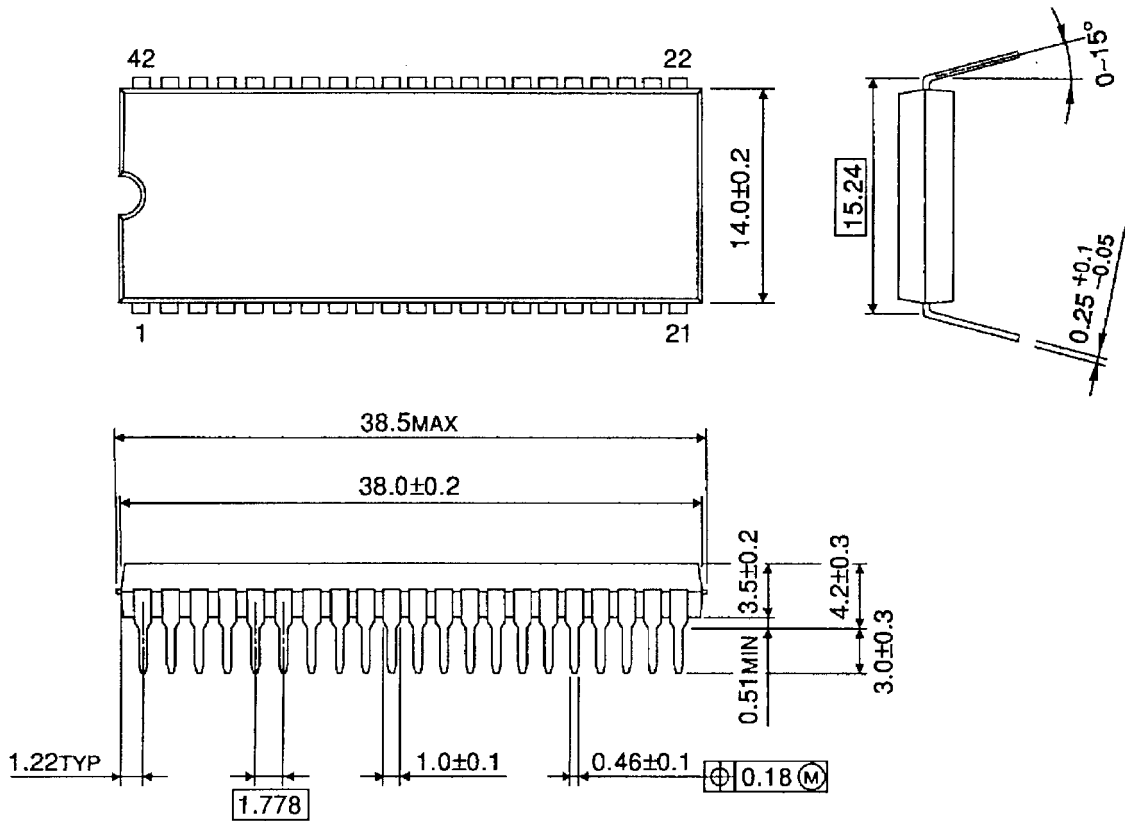
Weight: 4.12 g (typ.)

RESTRICTIONS ON PRODUCT USE